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Controlled Nucleation of Silicon Nanocrystals on a Periodic Template

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ABSTRACT

This paper presents a successful unification of standard lithographic approaches (top down), anisotropic etching of atomically smooth surfaces, and controlled crystallization of silicon quantum dots (bottom up) to produce silicon nanoclusters at desired locations. These results, in combination with our previous demonstration of Si nanocrystal uniformity in size, shape, and crystallographic orientation, show strong potential for the application of silicon nanocrystals in electronic devices.

To make a commercially viable electronic technology based on self-organized nanocrystals, the position of each nanocrystal must be controlled over a large area. Nanocrystal arrays with random positions are interesting demonstrations of crystallization techniques, but are impossible to individually contact with current device technology. Lateral ordering of III−V nanocrystals by the self-organization of strained layers in nonlattice-matched material systems has been demonstrated, but the nanocrystals are not compatible with the commercial ultra-large-scale integration (ULSI) and processing infrastructure and have poor long-range order.[1] Chemical methods of arranging nanoparticles within two-dimensional polymer matrices have also been demonstrated;[2,3] however, the long-range order and stability of these structures is not yet of device quality. This letter discusses a new and promising method of forming isolated silicon nanocrystal arrays using a combination of standard silicon processing technology and self-organization.

We have studied the properties of nanocrystalline silicon (nc-Si)/SiO_2 superlattices formed by thermal crystallization of amorphous silicon (a-Si)/SiO_2 layers and have produced silicon nanocrystals with uniform size and shape within this structure.[4] The a-Si/SiO_2 superlattices are formed by depositing alternating layers of a-Si and SiO_2 in an rf magnetron sputtering system by sputtering and plasma oxidation of a silicon target. A typical superlattice contains 4 to 20 periods with 25−60 Å SiO_2 and 20−250 Å a-Si layers. The a-Si layers are typically crystallized using a two-step crystallization procedure consisting of a rapid thermal anneal (RTA) at 900 °C for 60 s followed by a 60 min furnace anneal at 1050 °C. The RTA has been proven to initiate nucleation of the silicon nanocrystals, whereas the slower furnace anneal allows further crystal growth.[5] Due to the low diffusivity of silicon in SiO_2, segregation of the amorphous SiO_2 and crystalline silicon phases occurs during crystallization, forming a nc-Si/SiO_2 superlattice with abrupt interfaces and layer roughness on the order of 3−4 Å, as demonstrated by small-angle X-ray reflection, low-frequency Raman scattering, atomic force microscopy, and TEM analysis.[6,7] Confinement of the nc-Si layers between the SiO_2 layers provides excellent nanocrystal size control normal to the surface and is responsible for an observed preferential (111) crystallographic orientation of the nanocrystals in the growth direction.[8] Although the periodic nature of the nc-Si/SiO_2 superlattice effectively controls crystallite features in the normal direction, within the plane of each nc-Si layer, the nanocrystal size, crystal orientation, and lateral isolation are less controlled.

This investigation has focused on an attempt to control the in-plane properties of the silicon nanocrystals by depositing the superlattices on a specially designed template substrate. This template consisted of an array of inverted pyramid-shaped holes with submicron two-dimensional (2-D) periodicity, formed in the surface of a (100) crystalline silicon wafer. Anisotropic etching along different crystallographic directions, as illustrated in Figure 1, was used to

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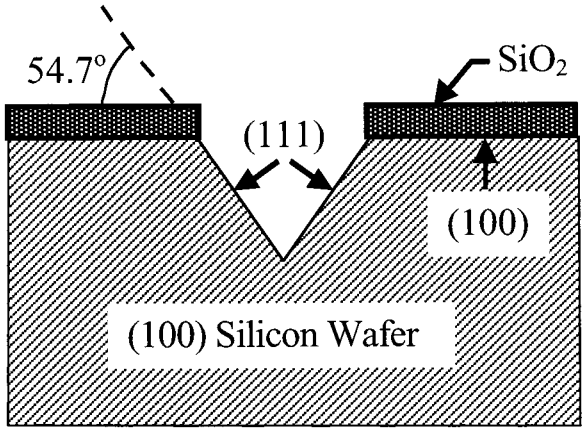

Figure 1. Potassium hydroxide (KOH) anisotropic etching of a silicon wafer will form inverted pyramid holes in areas not protected by an SiO_2 mask. The walls of each hole are formed by the (111) silicon crystal planes and are nearly atomically smooth.

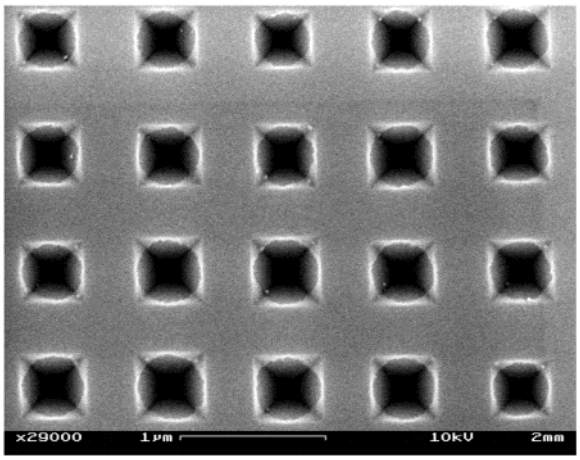

Figure 2. In this SEM image, several inverted pyramid holes are visible in a silicon wafer substrate after KOH etching. The circular ring within each square hole is the edge of the SiO_2 mask used to control the etched hole locations.

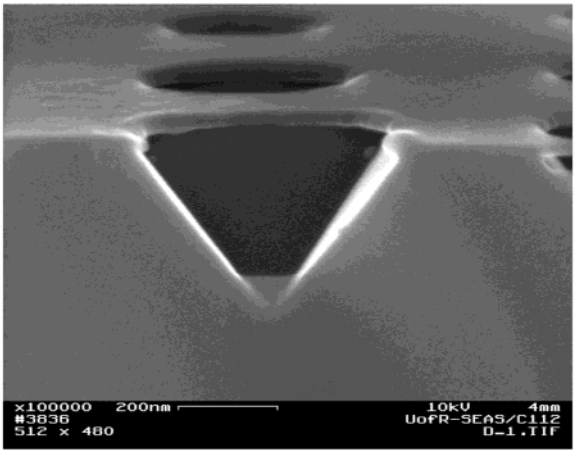

Figure 3. The sidewalls of the inverted pyramid holes are extremely smooth, as illustrated in the SEM image. The SiO_2 mask is also visible on the wafer surface.

form inverted pyramid holes with extremely smooth (111) sidewalls. We then studied how this three-dimensional template effected the nucleation of silicon nanocrystals in a-Si/SiO_2 superlattices.

The base material for the template was a (100) n-type 5 Ω-cm silicon wafer with a dry, thermally grown 300 Å SiO_2 layer. SiO_2 is resistant to anisotropic KOH chemical etching and therefore served as the masking material during the formation of the pyramid holes in the underlying crystalline silicon wafer.

To pattern the SiO_2, a maskless photolithographic technique called interferometric lithography was applied. With interferometric lithography, the interference pattern formed by the overlap of two laser beams is used to expose simple periodic structures in a photoresist layer.[9,10] Using this simple technique, large-area submicron arrays of holes with adjustable periodicity were formed in a 400-nm thick Shipley 1805 photoresist layer that was spun onto the SiO_2 layer. The 2-D arrays of holes were formed from the one-dimensional (1-D) interference pattern by exploiting the exposure memory of the photoresist. Each sample was partially exposed with the 1-D laser interference pattern, rotated by 90°, and partially exposed again. By properly timing this double exposure process, only those regions exposed twice at the peak interference intensity became fully exposed, while all other areas remained underexposed. During development, only the fully exposed regions of the photoresist were removed, forming a 2-D periodic pattern of holes in the film. This photoresist pattern was then transferred to the underlying oxide layer using reactive ion etching in a CHF_3/O_2 atmosphere.

With the oxide mask completed, the samples were then anisotropically etched in a 25% KOH solution at 70 °C for 3 min. Since the etch rate in the (100) direction is about 100 times faster than in the (111) direction,[11] the resulting (111) surfaces of each hole are nearly atomically smooth. Because four intersecting (111) crystal planes define each hole, the etch will always form rectangular-shaped holes when viewed from above, regardless of the shape of the masking holes. In Figure 2, an SEM image of several inverted pyramid holes is shown after KOH etching. In this image, the original SiO_2 mask is observable as the circular holes covering the square pyramid holes in the substrate. Figure 3 is an SEM cross section of a single pyramid hole in the substrate, with the SiO_2 mask also clearly visible on the surface.

After the residual oxide was removed by dipping the sample in a hydrofluoric acid solution, a 10 period a-Si/SiO_2 superlattice was deposited. The a-Si layers were each 50 Å thick, whereas the SiO_2 layers were 30 Å thick. Both films were sputtered using a Si target and argon plasma, with oxygen added to facilitate plasma oxidation during the SiO_2 deposition. The sample was then subjected to an RTA at 900 °C for 30 s to initiate crystallite nucleation. No furnace anneal was conducted on these samples because our goal was to study the effect of the 3-D template on crystallite nucleation.

Transmission electron microscopy (TEM) analysis of these samples revealed several interesting features. Figure 4 shows a TEM cross-section of a single inverted pyramid. From this image we can confirm that the superlattice remains intact as

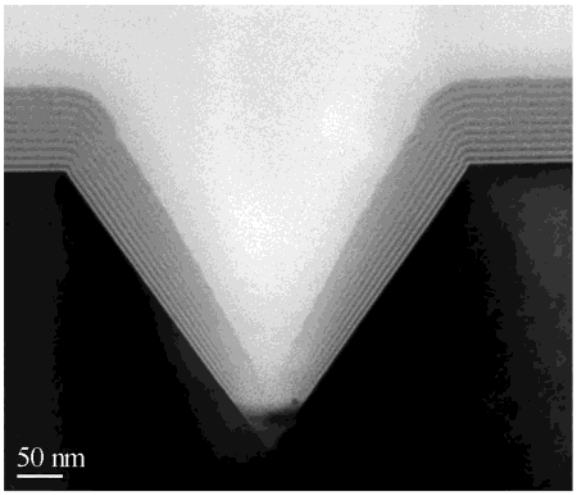

Figure 4. This TEM cross-section illustrates how the deposited a-Si/SiO_2 superlattice conforms to the substrate and gradually becomes thinner near the tip of the inverted pyramid. Near the tip, a small, round nanocluster can be seen just above the dark shadow cast by a portion of the crystalline silicon sidewall. This shadow also illustrates the difficulty involved in imaging this structure because the exact tip of the pyramid is extremely small and difficult to observe in a thin TEM cross-sectional sample.

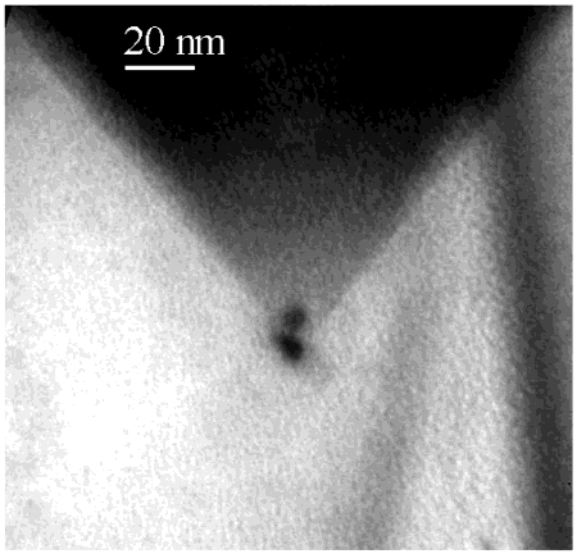

Figure 5. Nanoclusters formed within the deposited layers near the tip of an inverted pyramid are shown in this TEM cross-section. No clusters were observed at or near the wafer surface.

continuous layers through the transition from the wafer surface to the pyramid sidewall and can be resolved nearly to the tip of the pyramid. A gradual thinning of the superlattice along the (111) pyramid wall is also evident with a total thickness of 66 nm near the surface and decreasing to approximately 40 nm near the tip. This effect is likely due to the isotropic nature of the atomic flux in the sputtering process since similar effects have been observed in other plasma deposition processes on inverted pyramid textured substrates.[12] Atoms to be deposited emerge from the plasma traveling with various trajectories, and areas deep within the pyramid hole see fewer of these atoms than positions closer to the surface. Therefore, the total atomic flux decreases with depth into the hole, uniformly reducing the total film thickness.

Another interesting feature common in these samples is the appearance of small isolated silicon nanoclusters near the tips of the inverted pyramids as seen in Figure 5. Similar nanoclusters were visible in other TEM images, indicating that they are common features within this sample structure. All nanoclusters were located either at the inverted pyramid tip or on the sidewall near the tip and are therefore a direct result of the template geometry. The region near the pyramid tip contains unique stress gradients and is also a location of superlattice instability due to the thinning of the deposited layers. The effect of mechanical stress on solid phase crystallization is still a matter of debate, but we believe that a small amount of compressive stress will favor crystallization due to the volume contraction typically observed during the crystallization of silicon from the amorphous phase.[13] In our structure, compressive stress is likely present because sputtering generally deposits intrinsically compressive films.[14] In addition, the coefficient of thermal expansion is nearly an order of magnitude larger in Si than in SiO_2,[14] leading to some compressive stress in the a-Si layer during the heating cycle of the RTA, when cluster formation is most likely to occur. These characteristics may favor the coalescence of atoms into nanoclusters and could explain why they are not observed in other portions of the sample. Preferential nucleation of silicon nanoclusters near the tips of the inverted pyramids can be used in the fabrication of large area arrays of individually addressable silicon quantum dots.

In conclusion, we have demonstrated a novel technique for placing silicon nanocrystals in specified locations on a silicon wafer using standard silicon processing technology. The pattern generated in this work could easily be integrated into a random access memory (RAM) device, since memory structures typically have a periodic row by column layout to simplify the addressing process. Based on the appearance of nanoclusters at the tips of the inverted pyramid holes in our template, we are optimistic that accurately positioned silicon nanocrystal arrays will soon be demonstrated using this technique.

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